



Front End Board - FEB

WBS 2.6.2

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Harvard University

CD-2 Review of NOvA
Electronics/DAQ breakout session
June 5, 2007



Outline

- Personnel
- FEB location & functionality
- Custom and semi-custom devices
- R&D plan
- Production & QA



Personnel

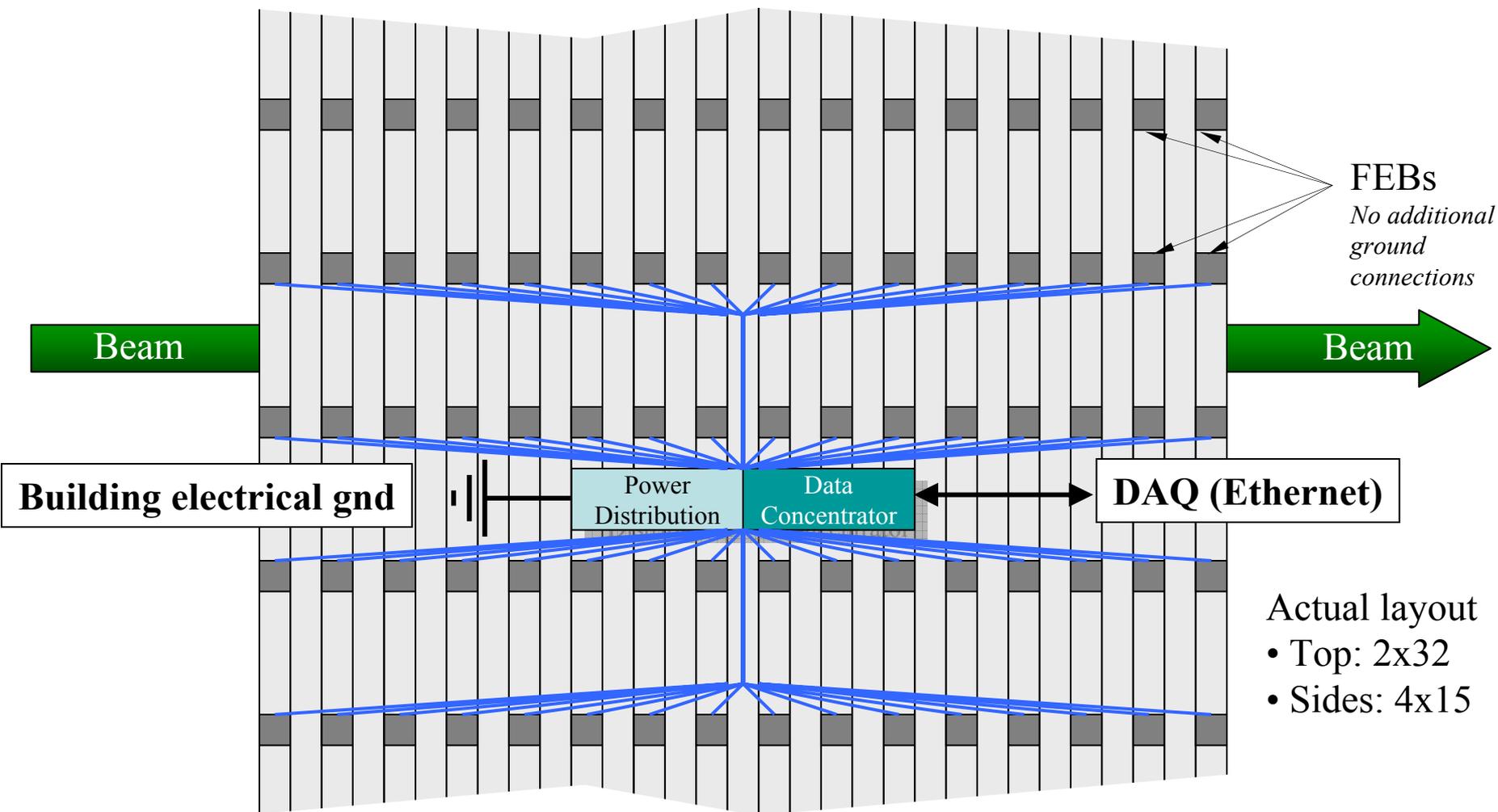
John Oliver, Nathan Felt, Sarah Harder, Josh Boehm, Steven Cavanaugh
-Harvard University –

Tom Zimmerman
- Fermilab -

Gerard Visser
- Indiana University-



On-Detector Electronics Distribution – Up to 64 per unit



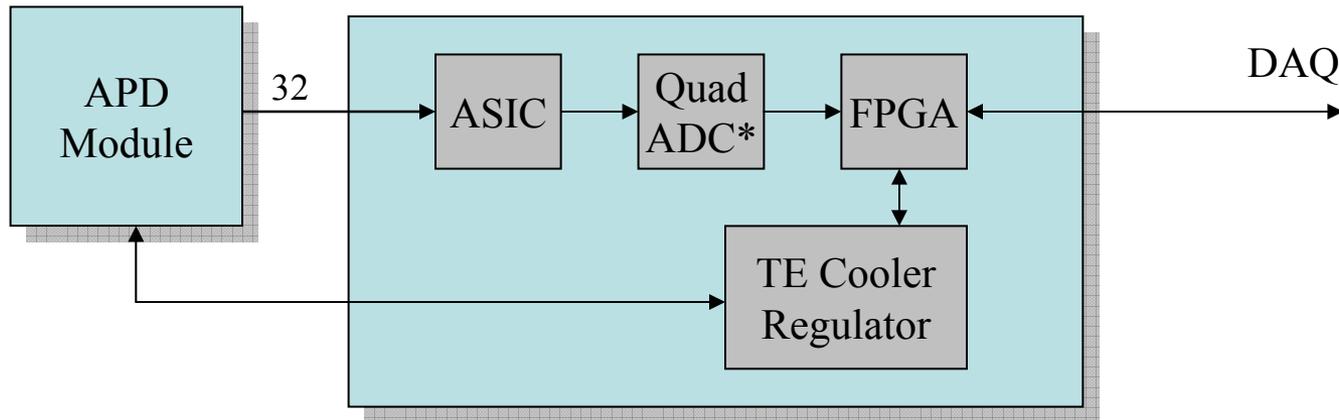


FEB Functionality

- Integrate APD signals and sample at 2 MHz : 32 pixels/board
- Low noise : < 200 e rms
- Real time clock for event timestamp
- Data driven signal processing
 - Pulse height extraction using multiple correlated sampling
 - Timing extraction – DSP techniques (matched filtering) for good timing resolution
 - Sparsify data : Time stamp, pulse height, address
 - 10 bytes per hit transmitted to DCM
- Estimated data rate (background) with 2x safety factor
 - ~ 240 Hz/pixel with few meters overburden
 - ~ 77 kB/s max per FEB (< 1.5 MB/s)
 - < 32 kB per spill “window” (~ 30 us)
 - Additional calibration data between spills
- In-situ calibration \rightarrow DSO mode
- TE cooler control
- Slow control monitoring
- 14,136 FEBs on NOvA Far Detector



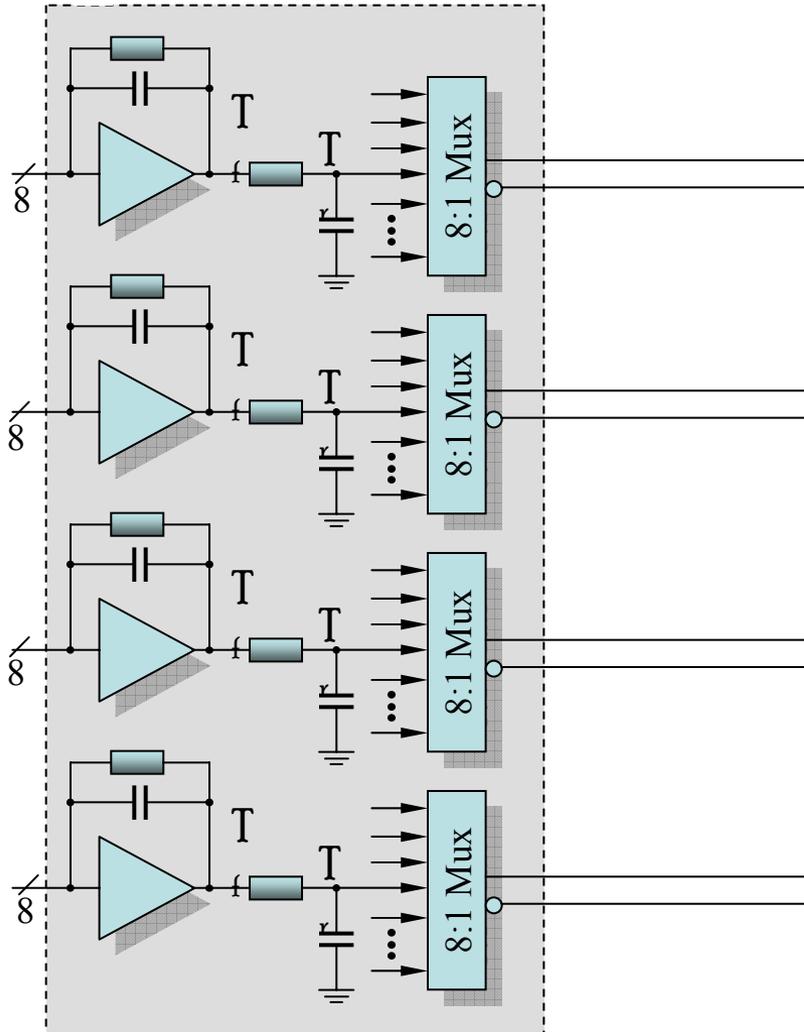
FEB Block Diagram



“Chipideas/CMS” AD41240



32 Channel Front End ASIC



- Tom Zimmerman - Fermilab
- 32 Ch. Integrator, shaper with programmable time constants
- enc < 200 e rms
- (4x) 8:1 Analog multiplexers
- Each runs at 16 MHz
- < 62.5 ns output settling time
- 500 ns equivalent sampling time
- 0.25 u TSMC CMOS
- FEB Ver 2.0 testing in progress but system “works nicely”



FPGA Functions

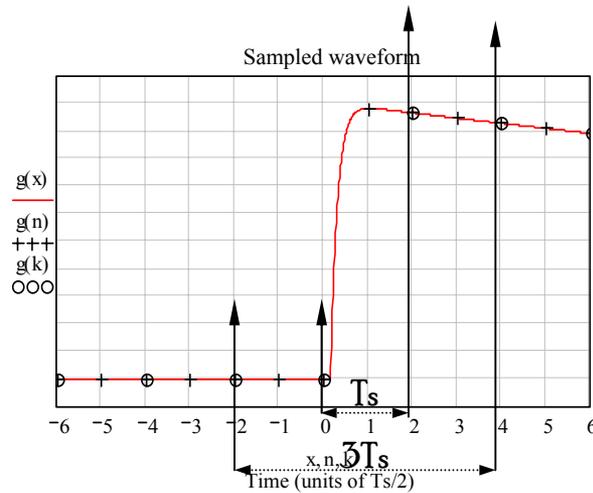
- Pulse height extraction
- Timing extraction
- Slow controls
 - Voltage, current,
 - TE cooler control
- i/o protocol implementation (Simple serial protocol, LVDS on Cat 5 cable)

Pulse height extraction

- Preliminary testing done with DCS (MASDA chip)
- FEB architecture allows for *multiple correlated sampling*
- For current (parallel) noise optimum number of samples is **two** .
- For voltage (series) noise, optimum number is **infinity**.
- Optimal number of samples and weights based on in-situ preamp measurements



Pulse-height extraction



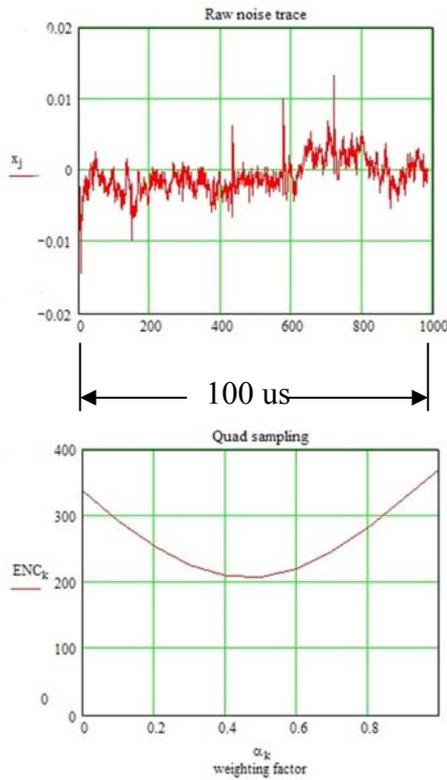
- Use multiple pairs of samples centered on leading edge
- Weight the pairs by optimal coefficients



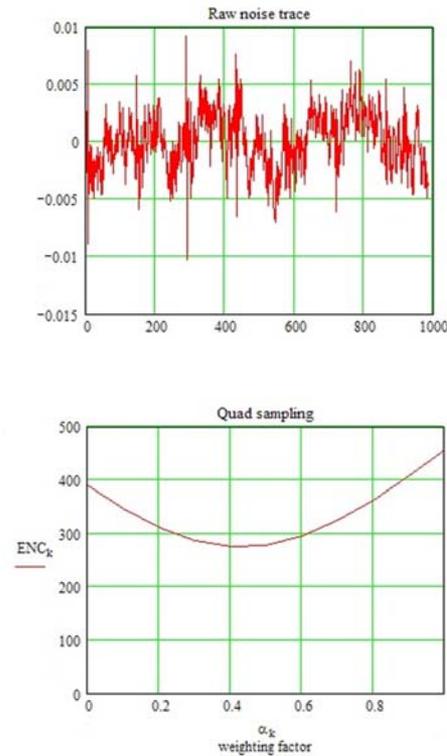
Noise filtering tests (Fall '05)

Example - Quad correlated sampling
(Based on tests with non-optimized preamp)

0 pf source



10 pf source



Note: spikes in signal are artifact of scope (chopper hv supply gets into preamp)



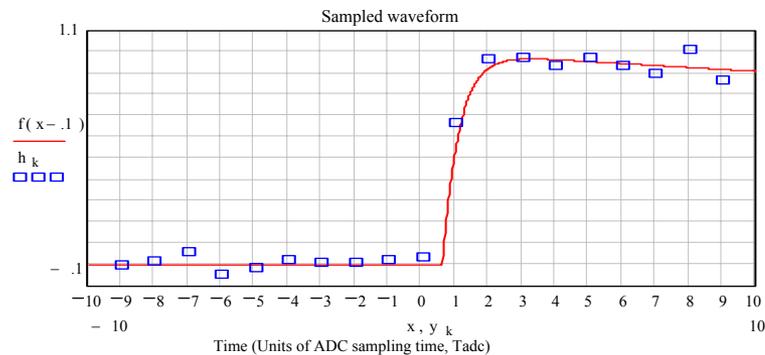
Timing extraction

- Simple identification of sampling time bin yields $500\text{ns}/\sqrt{12} = \sim 150\text{ns rms}$
- Multiple sampling and matched filtering¹ improves by $\sim 3 - 5$ depending on pulse height.
- We anticipate time stamping in 62.25 ns or 31.125 ns bins based on 16 MHz clk.

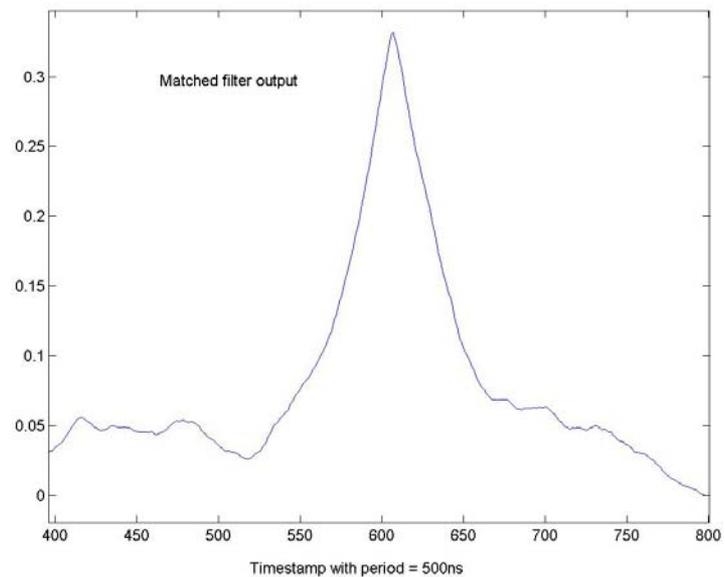
¹ Matched filter \rightarrow convolution of signal with ideal pulse shape followed by “interpolation” algorithm



Timing Extraction

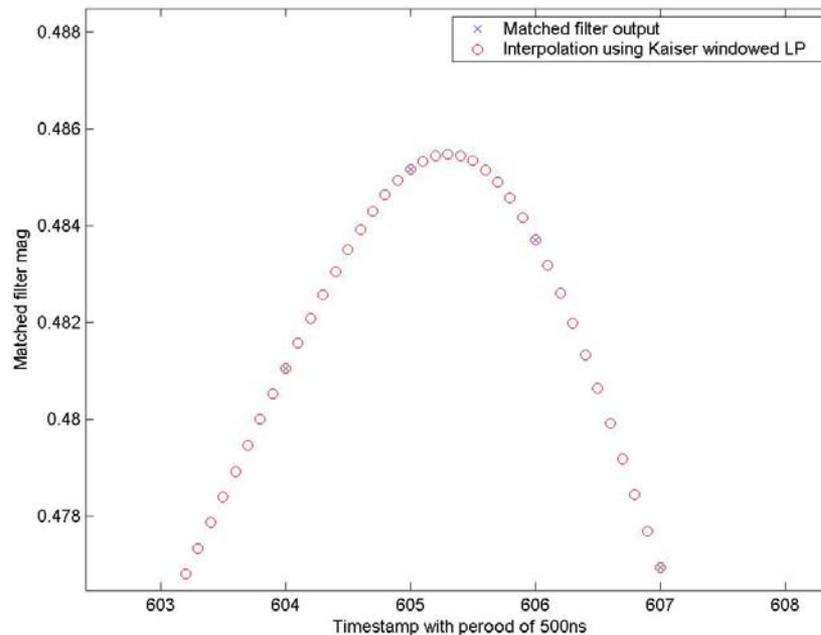


Matched filter output





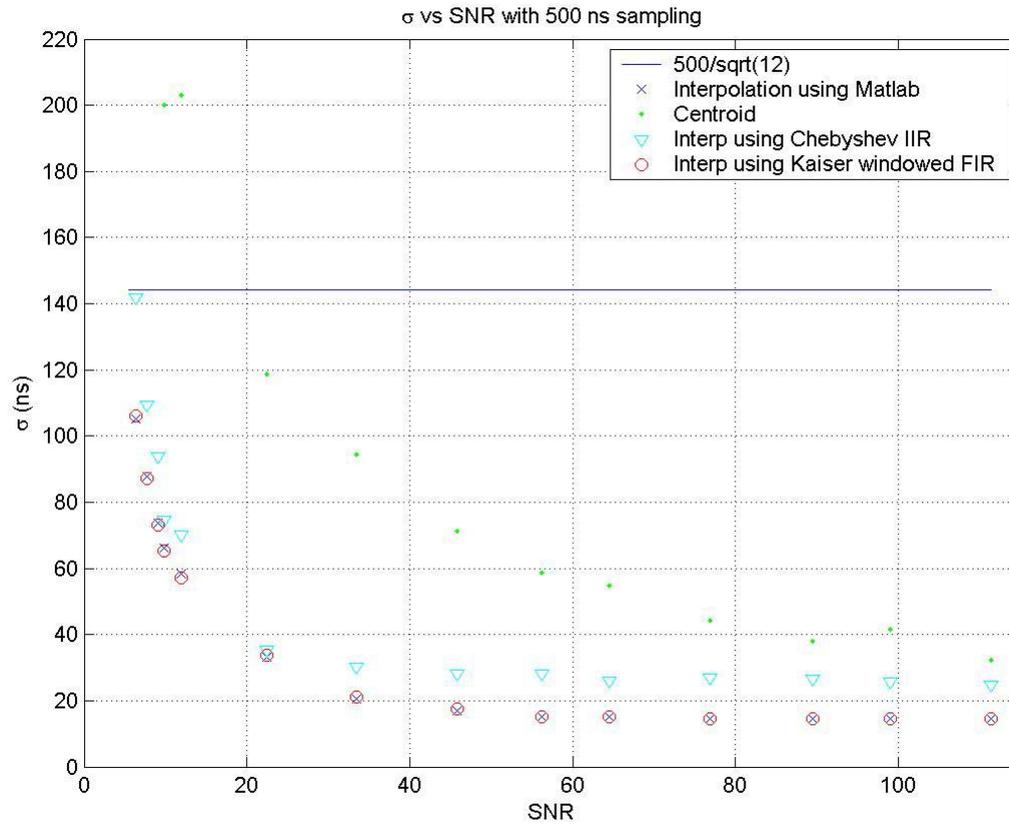
- Interpolate between samples using sinc function ($\text{sinc}(x)=\sin(x)/x$) (Shannon's interpolation theorem)
- In example below, interpolation is 10:1 (50ns point) – N. Felt



~ 40 samples used in convolution/interpolation (~ 20 us pulse history)



Timing resolution results (various interpolation methods)





FEB - Development

- Preliminary DSP tests for timing & Pulse-height extraction – Completed 2005
- Series of 4 prototype FEBs (under 1.6.2)
 - #1
 - Certification of AD41240* (4 ch, 40 Ms/s, 12-bit, custom ADC as used by CMS/HCAL – “Chipideas” Corp.) on FEB @ 16 Ms/s
 - Firmware development
 - USB interface
 - No ASIC
 - No interface to APD module or TE cooler
 - No interface to Data Concentrator
 - Currently under test
 - #2 (Currently under test)
 - Add ASIC & interface to APD module
 - Firmware development (con’t)
 - Add TE cooler controller
 - Retain USB
 - Detector “ready” – 10 copies produced



Development Plan – con't

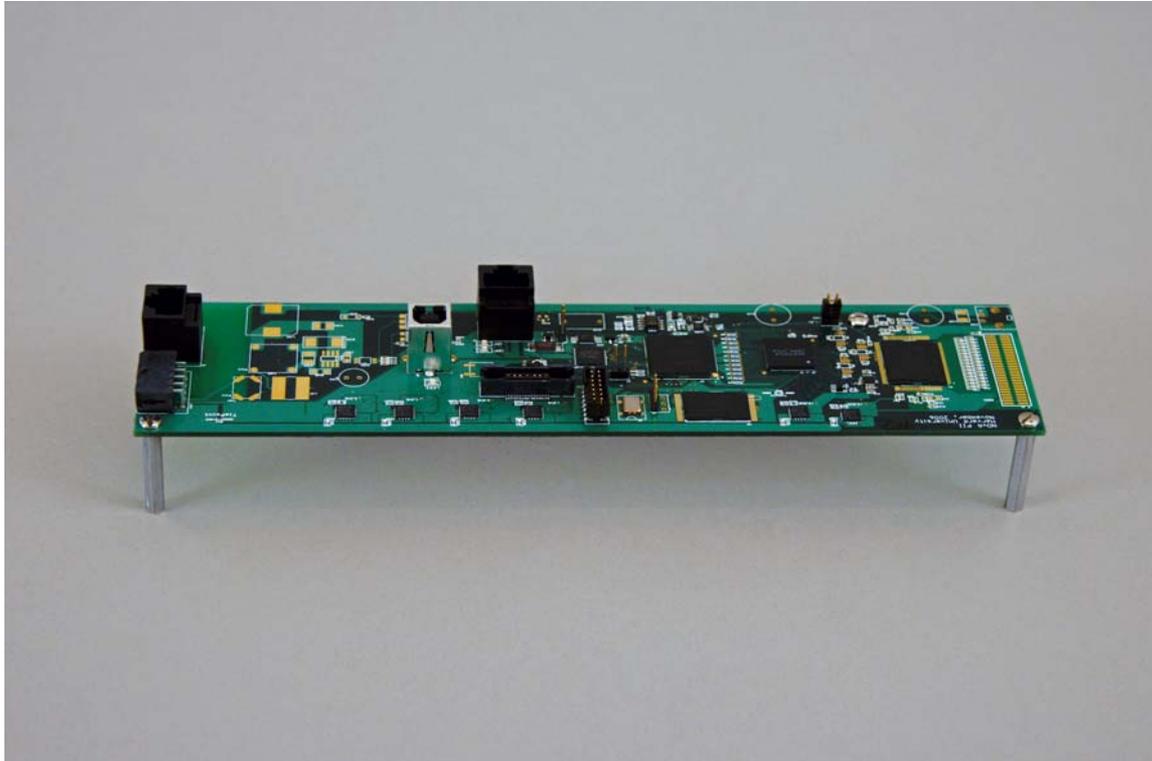
- #3
 - Replace USB with DAQ interface to Data Concentrator Module (DCM)
 - Firmware development (con't)
 - Detector “ready”

- #4 (May merge with ver 3.0)
 - Final production ready prototype
 - Firmware development (con't)
 - To be produced in qty ~ 400 for Integration Prototype Near Detector (IPND)

- See wbs for cost/manpower details



FEB 2.0

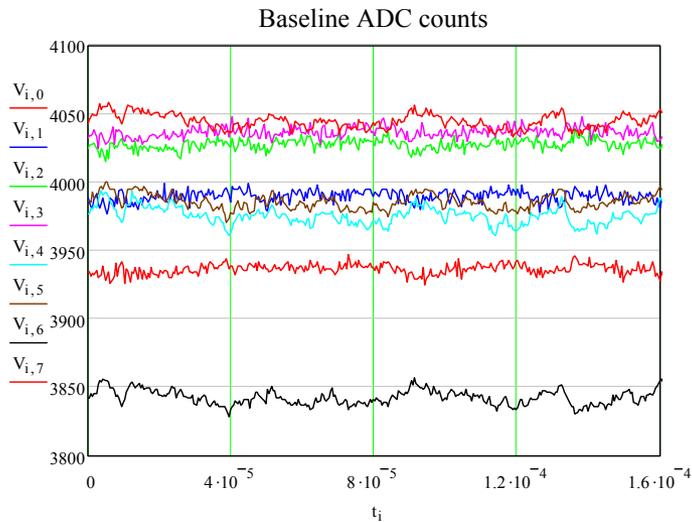




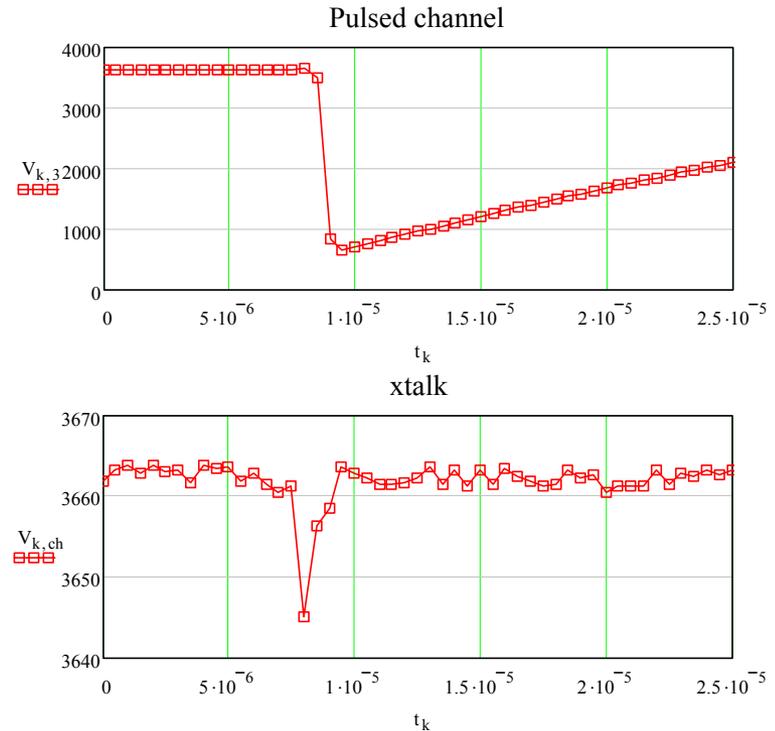
FEB Ver 2.0 testing

- DSO mode : 500 samples/channel @ 500ns/sample = 250 ms

Data for noise measurement



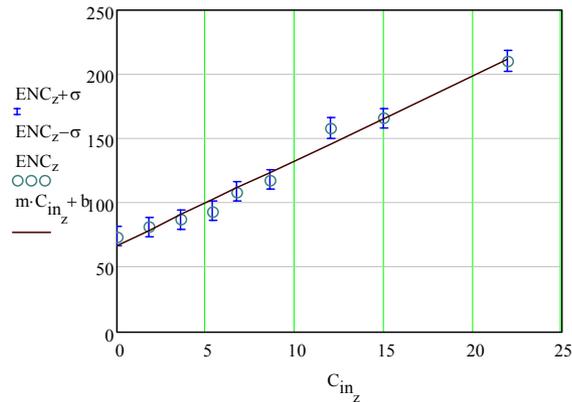
Data for xtalk measurement



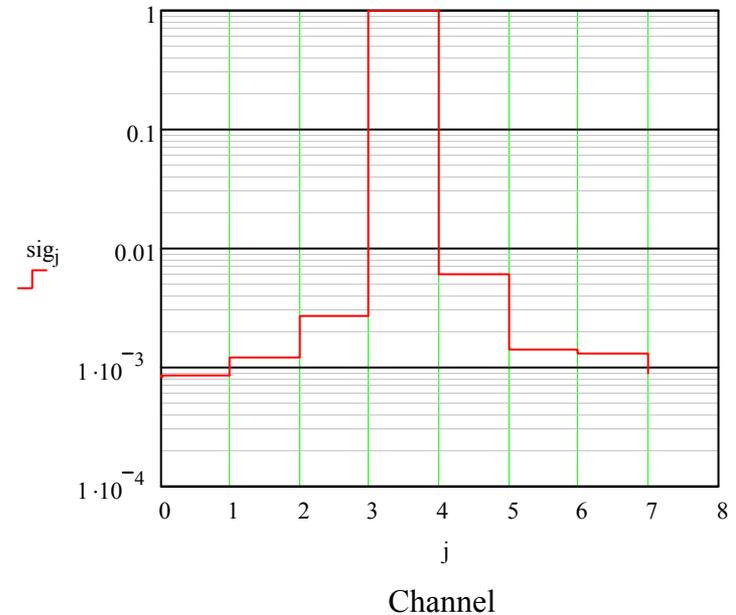


Some FEB 2.0 test results

ENC vs C_{in} ($I_{bias} = 1\text{ma}$, $T_r=190\text{ns}$)



Normalized crosstalk



- Based on DCS
- Above data taken with no APD
→ No leakage current
- Multiple sampling algorithm to be optimized in-situ to optimize leakage and preamp noise

- $\text{xtalk} < 0.7\%$ nearest neighbor
- $\text{xtalk} < 0.02\%$ other channels
- Should be highly suppressed by DSP triggering algorithms



ASIC development

- TSMC 0.25u CMOS
- Responsibility - Fermilab/ Tom Zimmerman
- 2 Prototype MPW runs in wbs
- Ver 1.0
 - Successfully benchtop tested at Fermilab
 - Successfully tested on FEB 2.0 at Harvard
- MPW run of ~400 pieces to be used on IPND



ASIC development – con't

- Ver 2.0
 - Under design @ Fermilab
 - Flexible architecture for Near & Far detectors
 - 8:1 multiplexing for Far detector
 - Near detector requires higher sampling rate to resolve overlapping events.
 - Higher sampling rate to be handled by “configurable” output multiplexer
 - 250 ns sampling \rightarrow (8x) 4:1 multiplexers, 8x differential outputs, 2x quad ADCs required
 - 125 ns sampling \rightarrow (16x) 2:1 multiplexers, 16x differential outputs, 4x quad ADCs required.
 - ASIC Ver 2.0 will have configurable output multiplexer to handle all three configurations
 - Target submission date \rightarrow Aug '07
 - Near Detector FEB will contain 4x quad ADC



FEB Production & QA

- ASIC → Fermilab : Custom test stand for packaged parts
- FEB → Harvard responsibility
- Recent large scale development/production experience at Harvard.
 - Front End Electronics for ATLAS Muon Spectrometer – MDT Chambers (Harvard/BU collaboration)
 - ~360,000 channels precision drift tubes
 - Developed 8-ch MDT-ASD chip (Amp/Shaper/Disc) in HP 0.5u CMOS
 - Production run of ~75k chips & ~16k Front End Boards
 - Developed high speed custom chip tester (~ 3 sec/chip full functional test with database entry)
 - Tested 75k chips > 1k/day limited by chip loading/unloading
 - Burned-in & tested 16k Front End Boards @ 150/day
 - Burn-in experience
 - ❖ Almost no failures observed during 24 hr burn-in
 - ❖ Failures occurred almost entirely at power up or not at all during burn-in period.
 - ❖ Test rate of 150/day limited by burn-in capability (1 full rack at elevated temp)
 - ❖ Conclusion: Burn-in not worth the trouble for NOvA.



FEB Production testing wbs-2.6.2

- Test stand
 - Concentrator
 - 64 APD modules
- 64 FEBs at a time
- 1 minute/FEB total install & uninstall (1 Hr)
- 30 min test (dominated by TE cooler control)
- Full functional test & database
- 2 hr cycle time
- ~ 250 /day /test stand
- With 1 - 2 test stands – Full QC << 6 mo