



NOVA Front End ASIC Development

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30-Sep-04

In this paper we will report on the discussions that have taken place about the plans for ASIC development for the front-end of the APD readout. This discussion began in the context of the wooden detector where two different approaches were considered to meet the needs of the

Several new pieces of information were included in these discussions. These were:

- 1) It has been established that there is sufficient precision in the timing of the MI ramp to allow for a prediction of the arrival time of the neutrinos to within 10 μ sec based on timing information available from the MI at least two seconds before the pulse.
- 2) The possibility of detecting supernovae with the totally active detector has been raised and studies are underway to establish if it is really viable. Results of these studies will begin to be available at the end of this year. Supernova (SN) signals last for several seconds and their detection would require that the readout be active for all, or at least a majority of the time between spills.
- 3) With the MASDA readout of the APD, which is not optimized for this application and which uses the Dual Correlated Sample (DCS) method, the total noise level observed at -15°C is ~ 300 electrons at the pre-amp input. The contribution of the APD dark current to this noise is ~ 100 electrons.
- 4) Studies performed by the Harvard group suggest that the electronics noise can be further reduced by $\sim 25\%$ by extending the DCS method to include more pre- and post-samples.

Three options were considered:

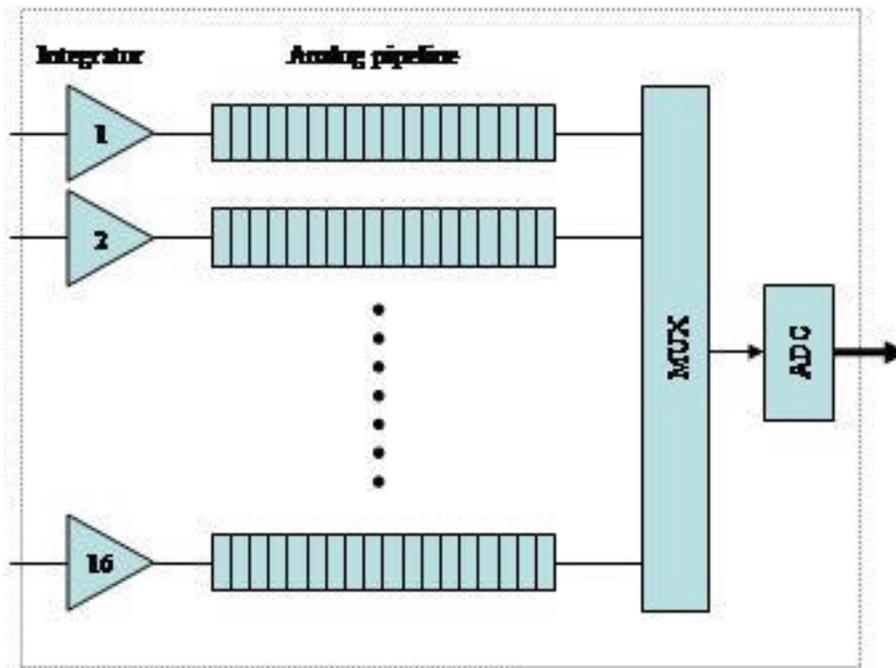
- 1) A low live-time readout optimized for the θ_{13} measurement.
- 2) One with a maximum of 50% live-time.
- 3) One with full or nearly full live time.

The objective in all three cases is to deliver digitized pulse heights for all time bins of interest to an FPGA where the correlated sampling and time stamping is performed. All of the three architectures would use digital signal processing performed off-chip in an FPGA.

In the first two cases, a reasonably accurate NUMI beam spill signal, arriving before the spill, is required. In option 3, it may or may not be required as discussed in a later section. In addition, options 2 and 3 are of interest mainly in the case that SN detection by the NOvA detector is possible.

1. Low live-time option

This consists of a 64-deep analog pipeline, sampled at 500ns intervals for a total of 32 μ s. The NUMI timing signal can be used to start a single fill the pipeline, or alternatively, simply to stop it at the appropriate time leaving the 10 μ s long beam spill events recorded within the pipeline.



At the end of the recording interval, the pipeline is read out by placing the sampling capacitors, in turn, onto the feedback loop of a sense amplifier. Thus one sense amplifier is required per pipeline. The output of the sense amplifier is converted to a digital signal with a Gray code Wilkinson ADC whose speed requirement is not critical. For this discussion was assumed to be about 4 $\mu\text{sec}/\text{sample}$ on average. The conversion of the signals from each of the 64-pipelines is done in parallel, so the average conversion time for the whole spill is ~ 250 microseconds.

Depending on the speed of the ADC, the live-time can be increased by taking non-beam spill data, but not higher than the 10% level. In any case, since ADC speed is not critical, cost savings may favor an on-chip gray-counter based Wilkinson type.

Pros:

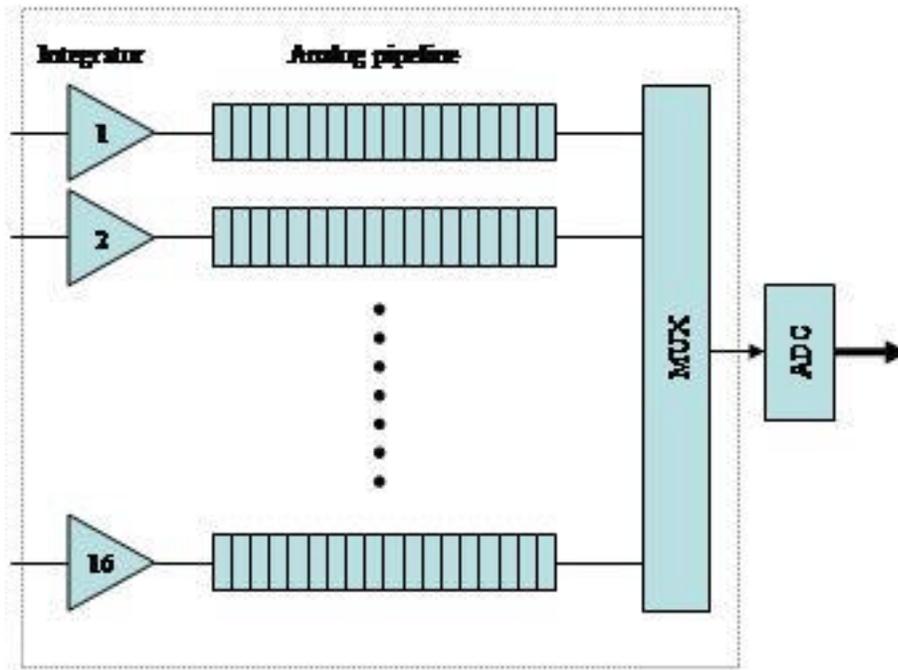
- 1) *This is a relatively simple chip to design, based on similar devices that have already been produced by the Fermilab group.*
- 2) *The signal acquisition and the digitization of the signal occur at different times.*

Cons:

- 1) *The low effective live-time would make it in-appropriate for SN detection.*
- 2) *Precision NUMI beam spill signal is required.*

2. 50% live time option

The architecture for this approach is similar to the low live-time option but uses a high speed external ADC as shown below.



In this case, the pipeline alternately records data then is read out by the ADC. As an example, a 40 MHz external ADC can digitize all channels (4096) in the 16 pipelines within 25 us resulting in a live time of:

$$\frac{32us}{(32 + 25)us} = 56\%$$

Since data recording and readout occur at different times, there will be no possibility of ADC or MUX related switching activity feeding through to the preamplifier front ends.

Pros:

- 1) *The signal acquisition and the digitization of the signal occur at different times.*
- 2) *Live-time fraction of ~ 55%.*

Cons:

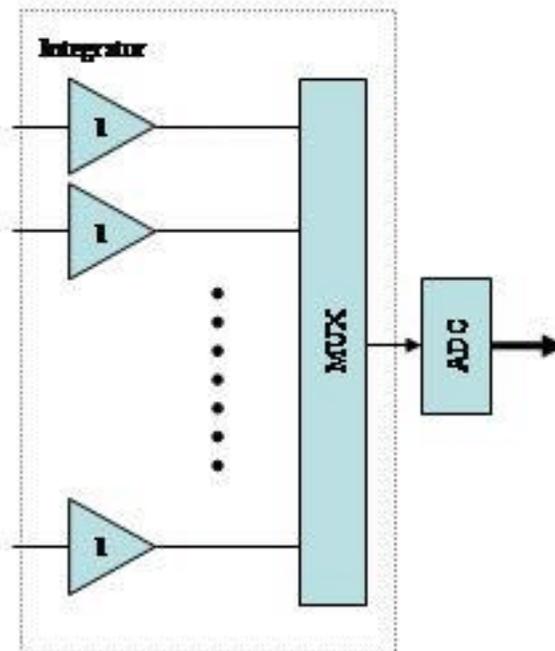
- 1) *Sense amplifier settling times:* The sense amplifier must acquire the sampled voltage in each cell within the allotted digitization time of the ADC (assuming the ADC has its own sample/hold circuit). If the pipeline is read out sequentially, this requirement can be relaxed somewhat, as lack of settling

appears as an additional time domain filtering on the signal. Still, the 0.1% (10 bit) settling time cannot be wildly different than the readout time per cell.

- 2) *Differential output stages*: Many commercial high speed ADCs have true differential inputs, a feature which offers a high degree of noise immunity and common mode rejection. To take advantage of this, the front end ASIC must deliver a true differential signal. Thus, a single ended to differential stage with common mode control (common mode feedback) must be designed.
- 3) *Precision NUMI beam spill signal is required.*

3. Full live-time option

The idea here is to continuously multiplex and digitize the signals with an external ADC so that each channel is digitized every 500ns. This requires that the multiplexer operate at 32 MSPS as shown in the diagram below.



Pros:

- 1) *100%, or nearly 100% live-time.*
- 2) *Less silicon real-estate required.* The switched capacitor arrays in options 1 and 2 are large. For this device the number of devices per wafer should be larger.

Cons:

- 1) *The signal acquisition and the digitization of the signal occur at the same time. This is thought to be the biggest risk factor associated with this readout. Feedback between the digitizer output and the pre-amp input will need to be suppressed to a level of ~ 50 electrons.*

- 2) *Preamp reset:* In options 1 and 2 the integrating capacitor will be reset by a reset FET switch. For 100% live-time an on-chip feedback resistor of order 40 M Ω is required. This is difficult to achieve in an ASIC process and techniques would have to be found or developed to achieve it. A reasonable alternative would be to use a preamp reset switch, as for options 1 and 2, activated after some fixed number of readout cycles and out-of-phase with the NUMI spill. A >99% live-time could be achieved in this way but at the expense of the extra complexity of the synchronization..
- 3) *MUX settling time:* While no sense amplifiers are required in this design, the multiplexer must operate at true ADC speed of 32 MHz. Since sequential pieces of data belong to different channels, multiplexer settling must be complete to the ten bit level in the allotted time, in this case, 33ns.
- 4) *A differential output with common-mode feedback is required to drive the amplified signal off chip to the ADC.*

Recommendations:

- 1) The design of option 1 should be started immediately. This design is optimized for the theta-13 measurement but is not suitable for supernova detection. The benefits of low risk match the need to quickly demonstrate that the whole detector concept is feasible. This should remain our baseline design until the viability of the supernova detection with the detector has been established and a realistic performance test has demonstrated option 3.
- 2) The design study of option 3 should be continued. The higher risk of this readout approach should not jeopardize process of proving the detector technology. However, the design can proceed along with the physics studies to understand of the supernova signal. The decision process here is 1) demonstration of proof-of-principle with the discrete prototype currently being tested at Harvard. 2) The design, layout and simulation of an ASIC should be started, which will be followed by an MPW run and a realistic performance test. If at any time during this process it is clear that the supernova signal is unlikely to work, then this effort should be put on hold. The timescale for this decision is later than the need for a working version of option 1 to demonstrate the viability of the detector. The engineering effort for this should, however, be on the project baseline.
- 3) The option 2 should not be pursued. In the event that option 3 proves impossible and that a supernova signal is possible then this approach should be reconsidered.